Crystalline zirconia oxide on silicon as alternative gate dielectrics

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Since the advent of the first integrated circuit, SiO₂ has been used as the primary gate dielectric. However, for SiO₂ below 20 Å, the leakage current rises to 1–10 A/cm²,¹ which requires significant power dissipation and will alter device performance. Therefore, some experts have claimed that silica-based electronic technology has approached its limits.¹–³ To reduce the leakage current, many materials with higher dielectric constant have been suggested as alternative gate dielectrics, such as Ta₂O₅,⁴–⁶ TiO₂,⁷ Y₂O₃,⁸ ZrO₂,⁹–¹¹ ZrSiO₄,¹² SrTiO₃,¹³,¹⁴ etc. Unfortunately, many of these materials are not thermally stable on silicon. The formation of SiO₂ or metal silicides often occurs when these materials are deposited on silicon or during subsequent annealing. Since SiO₂ has a lower dielectric constant, an underlying SiO₂ layer can reduce the effective capacitance of the film. In addition, the amorphous SiO₂ on silicon leaves dangling bonds that may result in electronic defects, disrupting transnalral symmetry at the interface.¹⁶ Ritala et al.³ had used a chemical approach to deposit amorphous oxide film on a silicon wafer without an interfacial silicon oxide layer. McKee et al.¹⁶ used one monolayer of strontium silicide to stabilize the interface with silicon, and obtained crystalline oxide on silicon in SrTiO₃/BST/SrSi/Si systems. Because the crystalline interface preserves a commensurate correspondence between physical structures of the dielectric film and silicon substrate, it does not cause so many electrical defects at the interface. However, to scale up to cost-effective production, a simple approach to grow a single crystalline high-κ layer on silicon is required for a feature-size reduction of the devices.

Yittria-stabilized zirconia (YSZ) (dielectric constant 25–29.7) is a very potential gate dielectric because of its high thermodynamical stability in contact with silicon even at 1000 K.¹⁷ And through the investigation of Schottky barrier heights and band offsets of various metal oxides by the theory of band lineups of semiconductors, Robertson¹⁸ concluded that ZrO₂ and ZrSiO₄ have sufficiently large electron barriers for use as alternative gate oxides. Here we report the growth and electrical properties of ultrathin crystalline YSZ films on silicon.

The YSZ thin films were grown on a native silicon wafer with the laser molecular beam epitaxy (MBE) technique. The deposition of initial several monolayers was in the base pressure of 10⁻⁶ mbar at 730 °C. The oxygen partial pressure was increased slowly up to 10⁻⁵ mbar and the deposition of YSZ was continued. The crystallinity of the films was in situ monitored by reflective high-energy electron diffraction (RHEED). After the deposition, the films were annealed at 700 °C for 10 s in reduced oxygen gas. Details of our systems have been reported elsewhere.¹⁹,²⁰

Figure 1 is a typical RHEED pattern of YSZ films grown on a silicon (100) wafer, where the bright streaky area indicates two-dimensional growth of a film with a smooth surface and the high degree of crystallinity of the film. An x-ray diffraction pattern of the films showed that the deposited films had single crystal orientation. An atomic force microscopy (AFM) investigation showed that the root mean square roughness of the deposited films was only about 0.3–0.5 nm, indicating atomically smooth films.

Figure 2 shows a cross-sectional transmission electron microscopy (TEM) image of 12.5 nm YSZ film deposited on a Si(100) substrate. YSZ films were found to grow epitaxially on the Si(100) substrate with crystal orientation correlation of YSZ(001)∥Si(001) and YSZ[100]∥Si[100]. Most obvious is that there is no amorphous interfacial oxide at the interface. The YSZ–Si interface is atomically sharp, within the region of imaging. But some misfit dislocations can be observed at the interface which are caused by the mismatch
of the lattice constant between YSZ and the silicon substrate. In general, the thickness of native amorphous SiO\textsubscript{2} on the surface of the Si wafer is about 1.0–1.5 nm. However, no amorphous SiO\textsubscript{2} layer was observed at the YSZ/Si interface in the cross-sectional TEM image. It implies that the native oxide layer had been removed by the bombardment of Zr ions, and the subsequently deposited YSZ film has sufficient stability and resistivity against the formation of an interfacial SiO\textsubscript{2} layer.

To confirm the elimination of silicon oxide in the YSZ/Si heterostructure, we conducted an x-ray photoelectron spectroscopy (XPS) investigation of the films. For reference, a native wafer gives Si 2\textit{p} spectra in Fig. 3(a), and Fig. 3(b) shows Si 2\textit{p} spectra of clean silicon. The native silicon oxide can be distinguished: a peak shifts 4.6 eV from that of clean silicon. Figure 4 is the depth profile of Si 2\textit{p} core-level spectra of 12.5 YSZ films on silicon. It can be observed that, with increasing depth, the intensity of the Si 2\textit{p} core-level spectra increased accordingly. But no peak corresponding to SiO\textsubscript{2} occurred at the interface. It suggests that there was no SiO\textsubscript{2} between the YSZ thin film and Si substrate, which is in agreement with the TEM image in Fig. 2.

Previously, we found that the partial pressure had a great effect on the interfacial state of the films.\textsuperscript{20} The lower pressure at the initial stage was beneficial for the formation of a crystalline interface. Therefore, we think there exists the following mechanism for the elimination of native SiO\textsubscript{2} and the formation of the crystalline interface during film deposition. Prior to the deposition, the thickness of SiO\textsubscript{2} on the substrate was in situ monitored by RHEED. From room temperature to the deposition temperature, the brightness of the RHEED pattern did not vary; this implies that the thickness of SiO\textsubscript{2} did not increase or decrease. In the deposition process the initial growth of several monolayers was conducted in oxygen partial pressure of 10^{-6} mbar at 730 °C, near the transition line from passive oxidation to active oxidation in the P–T phase diagram of silicon oxidation.\textsuperscript{21–23} Due to the shortage of oxygen in the chamber, the following chemical
The C–V curve of the film shows negligible hysteresis, indicating few unstable-trapped charges in the dielectric film. According to the Terman method, the interface state density can be extracted by comparing the ideal high-frequency C–V curve with the experimental curve, which gave a value of less than $2 \times 10^{11} \text{eV}^{-1} \text{cm}^{-2}$. As to the slight deviation of the C–V curve from the ideal ones in the accumulation region, we think it was caused by gate leakage and series resistance.

The leakage current of YSZ film is shown in Fig. 5. At 1.0 V bias, the leakage current is $1.1 \times 10^{-3} \text{A/cm}^2$. Although a direct comparison with SiO$_2$ is difficult due to different electrodes, the leakage is at least three orders of magnitude lower than that for SiO$_2$ with the same electrical thickness.

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