RHEED AND XPS STUDIES OF THE DECOMPOSITION OF SILICON DIOXIDE BY THE BOMBARDMENT OF METAL IONS

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In this paper, we report the RHEED and XPS studies of the decomposition of silicon dioxide by the bombardment of metal ions and the growth of ultrathin crystalline zirconia oxide film on silicon. Through XPS analysis, it was found that silicon dioxide could be decomposed by the bombardment of Zr ions in high temperature and lower partial pressure. Silicon dioxide was decomposed into evaporated silicon oxide, while part of the oxygen in silicon dioxide reacted with metal Zr ions to form stable zirconia oxide film. The metal ions reacted with silicon dioxide homogenously. Because of the smoothness of native silicon dioxide surface and atomically abrupt silicon dioxide interface with silicon, native oxide layer on silicon wafer was evenly removed and a sharp stable crystalline zirconia oxide interface with silicon was formed. The crystalline yittria-stabilized zirconia oxide (YSZ) film with equivalent electrical oxide thickness 1.46 nm show excellent electrical properties, the interface state density less than $2 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ and leakage current $1.1 \times 10^{-3}$ A/cm$^2$ at 1.0 V bias. It demonstrates that this method can be used to the deposition of high-$\kappa$ metal oxide as alternative dielectrics for future generation device.

1. Introduction

Ultrathin silicon dioxide (SiO$_2$) thermally grown on silicon has been used as primary gate dielectric materials in metal-oxide-semiconductor field-effect device (MOSFET) since the advent of the first integrated circuit. However, as device scaling continues, one of the more fundamental limits to the scaling of gate dielectric is the exponential increase in tunneling current with decreasing film thickness. To reduce the leakage current while maintaining the same gate capacitance, many materials with a higher dielectric constant have been suggested that could replace SiO$_2$ as possible gate dielectrics, such as Ta$_2$O$_5$, TiO$_2$, Y$_2$O$_3$, ZrO$_2$, ZrSi$_2$O$_x$, and SrTiO$_3$ etc. Unfortunately, the formation of SiO$_2$ or metal silicides often occurs when these materials are deposited on silicon or during subsequent annealing. Since SiO$_2$ has a lower dielectric constant, an underlying SiO$_2$ layer can reduce the effective capacitance of the film. In addition, the amorphous SiO$_2$ on silicon leaves dangling bonds that may result in electronic defect, disrupting translational symmetry at the interface. Therefore, a simple approach to growing single crystalline high-$\kappa$ layer on silicon without the formation of underlying SiO$_2$ layer is required for the feature-size reduction of device.
In a previous paper,\textsuperscript{12} it was found that the partial pressure at the initial deposition stage is a major reason for the formation of the underlying SiO$_2$ layer. Therefore, how to remove the initial SiO$_2$ layer is very important for obtaining crystalline layer on silicon. There are two conventional ways to remove the SiO$_2$ layer on the silicon wafer. One is that silicon surface is etched with a dilute aqueous HF solution to leave the surface hydrogen-terminated. But Copel \textit{et al.}\textsuperscript{6} found that ultrathin ZrO$_2$ films grown on the HF stripped silicon wafer nucleate as island with rough interface. Another is the thermal annealing of silicon wafer in high temperature and ultrahigh vacuum, resulting in decomposition of oxide layer. However, the oxide layers decompose inhomogeneously accompanying with the void formation on the clean silicon surface.\textsuperscript{13--17} The thermally induced defects around the Si/SiO$_2$ interface is one of key issues to achieve good electrical reliability in the MOS devices. In this report, we removed SiO$_2$ by the bombardment of Zr ions in high temperature and lower partial pressure. While the oxygen in the SiO$_2$ layer was used as oxygen source to react with metal Zr ions to form initial several YSZ monolayers. The metal ions react with silicon dioxide homogeneously. Because of the smoothness of SiO$_2$ surface and atomically abrupt SiO$_2$ interface with silicon, the oxide layer on silicon wafer was evenly removed and a sharp stabilized crystalline zirconia oxide interface with silicon was formed. Due to the thermodynamically stability in contact with silicon and strong resistivity to oxygen interdiffusion, ultrathin crystalline YSZ films were grown on silicon without the formation of SiO$_2$ layer at the interface.

2. Experimental

Experiments were carried out in a chamber with base pressure in the $10^{-7}$ mbar range. The chamber was equipped with reflective high-energy electron diffraction (RHEED) to \textit{in situ} real monitor the surface smoothness and crystallinity of the silicon substrate and deposited films. The YSZ thin films were grown on native silicon wafer with the laser MBE technique. The Si substrates were cleaned in acetone, ethanol and rinsed in distilled water. After loading into the substrate, the chamber was evacuated down to $10^{-7}$ mbar. Then the substrate was heated slowly to 730$^\circ$C. The deposition of YSZ was in the base pressure of $10^{-6}$ mbar and 730$^\circ$C, which is intended to remove SiO$_2$ layer and to obtain stabilized crystalline interface. Details of our systems have been reported elsewhere.\textsuperscript{12,18} Parts of as-deposited ultrathin films were rapid-thermal-annealed (RTA) in reduced pure oxygen gas for TEM and electrical properties characterization, and the annealing time was carefully adjusted for about 10 s so that no amorphous interfacial SiO$_2$ layer formed. The interface was investigated by using high-resolution transmission electron microscopy (HRTEM) in a Philips CM 300 operating at 300 kV accelerating voltage, which has a point-to-point spatial resolution of 1.7 Å. X-ray photoelectron spectroscopy (XPS) investigation was performed in a VG ESCALAB 220I-XL system, using Mg K$\alpha$ as X-ray source. The capacitance–voltage (C–V) and current–voltage (I–V) measurements were taken by the standard method at HP 4192A and HP 4155B analyzers. Al dots 1 mm in diameter were evaporated on the oxide surface as electrode.

3. Results and Discussion

Figure 1 shows the change in the RHEED spot intensity of native silicon wafer before the YSZ deposition. Figure 1(a) is the RHEED pattern of native silicon wafer at room temperature. After loading the silicon substrate into the chamber and evacuating the chamber down to $10^{-7}$ mbar, the substrate was heated slowly to 730$^\circ$C and the chamber partial pressure was adjusted to $10^{-6}$ mbar, above the transition line from passive oxidation to active oxidation in the P–T phase diagram of silicon oxidation but below the desorption line of SiO.\textsuperscript{19--22} Figure 1(b) is the RHEED pattern of native silicon wafer at 730$^\circ$C; the spot intensity is same as that of the RHEED pattern at room temperature. It can be seen that the silicon surface only slightly oxidized; this had been confirmed from the XPS results discussed in the following.

Figure 2 shows the XPS wide-scan spectra taken from native wafer without YSZ deposition, Figs. 2(a) and 2(b), and with YSZ deposition, Figs. 2(c)–2(f). The spectra show only Si, C and O elements for samples without YSZ deposition, with no other element being detected. For the samples with YSZ deposition, Si 2p peak intensity is clearly decreased relative to the Zr 3d peaks with YSZ deposition.
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Fig. 1. RHEED pattern of native silicon wafer at room temperature (a) and at 730°C (b).

Fig. 2. XPS wide-scan spectra of samples without YSZ deposition (a, b) and with YSZ deposition for 5 s (c), 10 s (d), 20 s (e) and 20 s (f), respectively.

Fig. 3. Si core-level spectra of samples without YSZ deposition (a, b) and with YSZ deposition for 5 s (c), 10 s (d), 20 s (e) and 20 s (f), respectively.

continuing. The Si 2p core-level spectra of samples are shown in Fig. 3. The native SiO$_2$ can be distinguished from the figure that a Si 2p0 peak at 103.6 shifts 4.3 eV from that of clean silicon Si 2p3 peak at 99.3 eV. For the native wafer without YSZ deposition, the intensity of Si 2p0 of native silicon wafer heated at 730°C is slightly stronger than that of native silicon wafer without heating. It implies that very little Si oxidized into SiO$_2$ on the surface of silicon, which may be due to the substrate temperature and chamber partial pressure near the transition line from passive oxidation to active oxidation in the P–T phase diagram of silicon oxidation.$^{19–21}$ After the YSZ deposition, the intensity of both Si 2p0 and Si 2p3 peaks reduced with the YSZ deposition. From Figs. 3(c) to 3(f) the Si 2p3 peak, corresponding to pure silicon, always presents in all the samples. It implies that the upper YSZ layers are thinner than X-ray photoelectron penetration depth and photoelectron can penetrate through the YSZ and interfacial SiO$_2$ layer and reach
pure silicon substrate. Therefore, the Si 2p0 peaks intensity decreasing from Figs. 3(c) to 3(f) suggest that the interfacial layer reduced with the YSZ deposition. Another obvious point in Fig. 3 is that after the YSZ deposition on substrate the distance between Si 2p0 and Si 2p3 peaks decreases with YSZ deposition, from 4.3 eV in Fig. 3(b) to 3.5 eV in Fig. 3(f). This suggests that the initial SiO2 layer was deoxidized into SiOx (x < 2) with YSZ deposition. Therefore, we think the reduction of the SiO2 layer is due to the decomposition of SiO2 with YSZ deposition. Previously, we found that the partial pressure had a great effect on the interfacial state of the films. The lower pressure at the initial stage was beneficial for the formation of crystalline interface. Therefore, we propose that there exists the following mechanism for the decomposition of interface SiO2 and the reduction of interfacial SiO2 layer with YSZ deposition. Prior to the deposition, the thickness of SiO2 layer on silicon substrate did not vary much. In the deposition process the oxygen partial pressure of 10−6 mbar and 730°C is near the transition line from passive oxidation to active oxidation in the P–T phase diagram of silicon oxidation. Due to the shortage of oxygen in the chamber, the following chemical reactions would take place when metallic Zr ions hit the wafer, which depended on the actual local condition of the Si wafer surface:

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\begin{align*}
\text{Zr (gas)} + 2\text{SiO}_2 & \rightarrow \text{ZrO}_2 + 2\text{SiO} \quad (\Delta G = -280.472 \text{ kJ/mole}) \\
-406.452 \text{ kJ/mole} & - 981.588 \text{ kJ/mole} - 1184.364 \text{ kJ/mole} - 326.349 \text{ kJ/mole}
\end{align*}
\]

\[
\begin{align*}
\text{Zr (gas)} + \text{SiO}_2 & \rightarrow \text{ZrO}_2 + \text{Si} \quad (\Delta G = -639.688 \text{ kJ/mole}) \\
-406.452 \text{ kJ/mole} & - 981.588 \text{ kJ/mole} - 1184.364 \text{ kJ/mole} - 30.39 \text{ kJ/mole}
\end{align*}
\]

Thus the atoms in the native amorphous SiO2 layer on the surface of Si wafer would be decomposed by the bombardment of metal Zr (or Y) ions. Rubloff et al.22 found that the critical oxygen partial pressure above which the SiO layer remains stable at 730°C is about 7 × 10−5 mbar. Thus the desorption of SiO, the reaction product, is expected for lower growth partial pressure of 10−6 mbar during YSZ deposition process. As a result, the thickness of amorphous SiO2 layer will be reduced or evenly eliminated in the lower partial pressure deposition process. While the oxygen in the SiO2 was used as oxygen source for the oxidation of YSZ films to form stabilized YSZ film on silicon.

According to the proposed decomposition mechanism above, we fabricated ultrathin crystalline YSZ layer on silicon without interfacial layer. Figure 4 shows a typical cross-sectional HRTEM image of 12.5 nm YSZ film deposited on Si (100) substrate. The YSZ films were found to grow epitaxially on Si (100) substrate with crystal orientation correlation YSZ(001) || Si(001) and YSZ[100] || Si[100]. The most obvious point is that there is no amorphous interfacial oxide observed at the interface. The YSZ-Si interface is atomically sharp, within the region of the image. But some misfit dislocations can be observed at the interface, which is caused by the mismatch of the lattice constant between YSZ and silicon substrate. In general, the thickness of the image. But some misfit dislocations can be observed at the interface, which is caused by the mismatch of the lattice constant between YSZ and silicon substrate. In general, the thickness

![Fig. 4. Cross-sectional HRTEM image of 12.5 nm YSZ film on Si(100) substrate. Commensurate crystalline interface of YSZ/Si heterostructure can be clearly distinguished and some misfit dislocations can be observed.](image-url)
of native amorphous SiO$_2$ on the surface of Si wafer is about 1.0–2.0 nm. However, no amorphous SiO$_2$ layer was observed at the YSZ/Si interface in the cross-sectional TEM image; it implies that the amorphous SiO$_2$ layer had been removed by the bombardment of Zr ions.

To confirm the elimination of silicon oxide in the YSZ/Si heterostructure, we conducted XPS investigation on the films. Figure 5 is the depth profile of Si 2p core-level spectra for ultrathin 12.5 nm YSZ films on silicon. It can be observed that, with the depth increasing, the intensity of Si 2p core-level spectra increased accordingly. But no peak corresponding to SiO$_2$ occurred at the interface. It suggests that there is no underlying SiO$_2$ formed between YSZ film and Si substrate, which is in agreement with the observation of TEM in Fig. 4.

The inset of Fig. 6 shows the high frequency C–V measurement for a 6.0 nm YSZ film at 100 kHz. The equivalent oxide thickness ($t_{eox}$) of 6.0 nm YSZ film is 14.6 Å, which was determined on the base of capacitance in the accumulation region. The C–V curve of film shows negligible hysteresis, indicating few instable-trapped charges in the dielectric film.

According to the Terman method, the interface state density can be extracted by comparing the high-frequency C–V curve with experimental curves, which gave the value of less than $2 \times 10^{11}$ eV$^{-1}$cm$^{-2}$. The leakage current of YSZ film is shown in Fig. 6. At 1.0 V bias, the leakage current is of $1.1 \times 10^{-3}$ A/cm$^2$. Although the direct comparison with SiO$_2$ is difficult due to different electrode, the leakage is at least three orders of magnitude lower than that for SiO$_2$ with the same electrical thickness.

4. In Summary

Through RHEED, TEM and XPS investigation, it was found that silicon dioxide could be decomposed by the bombardment of Zr ions at high temperature and lower partial pressure. Silicon dioxide was decomposed into evaporated silicon oxide, while part of the oxygen in silicon dioxide reacted with metal Zr ions to form stable zirconia oxide film. The obtained crystalline YSZ film without underlying amorphous SiO$_2$ have sharp interface with silicon. Crystalline YSZ film on silicon with equivalent electrical oxide thickness 1.46 nm show excellent electrical properties, the interface state density less than $2 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ and leakage current $1.1 \times 10^{-3}$ A/cm$^2$ at 1.0 V bias. It demonstrates that this method can be used to the deposition of high-$\kappa$ metal oxide as alternative dielectrics for future generation device.
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